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BEFORE THE BOARD OF PATENT APPEALS

AND INTERFERENCES

Paper No. 26

Application Number: 09/146,259

Filing Date: September 3, 1998

Appellant(s): Yoshida et al.

Ellen Marcie Emas

For Appellant

EXAMINER'S ANSWER

This is in response to the supplemental appeal brief filed October 17, 2002.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The appellant's statement in the brief that certain claims do not stand or fall together is not agreed with because they have failed to present reasons why their claims do not stand or fall together. 37 CFR 1.192(c)(7) states the following. "For each ground of rejection which appellant contests and which applies to a group of two or more claims, the Board shall select a single claim from the group and shall decide the appeal as to the ground of rejection on the basis of that claim alone unless a statement is included that the claims of the group do not stand or fall together and, in the argument under paragraph (c)(8) of this section, appellant explains why the claims of the group are believed to be separately patentable. **Merely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable.** Appellants have merely pointed out the differences in what the claims cover.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

5,815,698	Holmann et al.	9/29/98

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which th applicant regards as his invention.

Claims 1-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Consider first that appellants have offered no definition for the term, "instruction", anywhere in their specification and that they have used the term in multiple inconsistent ways throughout their disclosure. For example, "In the **instruction** formats, there are included a format 101 of dual operation instruction which designates two **operations** by one **instruction** word as shown in Figure 2a and a format 102 of single **operation instruction** which designates one **operation** by one **instruction** word as shown in Figure 2b" (p. 21, line 27 through p. 22, line 6), or "In this program, a pair of **sub-instructions** in each row is described by a dual **operation instruction** 101 having the instruction format shown in Figure 2a, wherein **sub-instructions** I01, I11, I21, I31, I41, I51, and I61 are described in the **operation** field 106 as **operation**_0 and **sub-instructions** I02, I12, I22, I32, I42, I52, and I62 are described in the **operation** field 107 as **operation**_1" (p. 50, line 5-12), or "The **sub-instruction** I01 is a branch **instruction** BRA ..." (p. 50,

line 18), or "The **sub-instruction** I21 is an add **instruction** ADD ..." (p. 50, lines 25-26), or "The **sub-instruction** I31 is a comparison **instruction** CMPEQ ..." (p. 51, lines 1-2). If one of ordinary skill in the art seeking to understand appellants' claims looks to appellants' specification, *supra*, for guidance as to how to determine what is an instruction, he gets only conflicting advice. A **branch** (BRA) is an **instruction** and also a **sub-instruction** (p. 50, line 18) which is equivalent to an **operation** (p. 50, lines 5-12). An (**instruction word**)/(VLIW instruction) can be either an instruction containing two **operations/sub-instructions** or an instruction containing one **operation/sub-instruction** (p. 21, line 27 through p. 22, line 6). This leads to the paradox where a **branch** (BRA) which is an **instruction** cannot be an **instruction word** though an **instruction word** is an **instruction**. **What part of applicant's original disclosure tells one of ordinary skill in the art that appellants did not mean instructions such as branches, compares, etc. when using the word instruction in their claims but instead meant instructions which are instruction words?**

Appellants have argued one of ordinary skill in the art would know that instruction word was meant by the term, "instruction", when used in their claims. Consider as a specific example the language of applicant's claim 21 when read in the light of appellants' specification.

The first phrase of claim 21, "A data processing device comprising", is generic to either interpretation of the word, "instruction".

The second phrase of claim 21, "an instruction decoder decoding a condition instruction to output a control signal", can be readily interpreted by p. 23, lines 16-20 of appellants' specification where it says, "In the instruction decode stage D/A, operation_0 described in the operation field 106 is decoded by the decoder 8 and operation_1 described in the operation field 107 is decoded by the decoder 9" and by p. 51, lines 11-16 of appellants' specification where it says, "On the execution condition field 401 corresponding to

the sub-instruction I01, there is described 'CC=010'; and sub-instructions other than the sub-instruction I01 are instructions executed unconditionally, wherein execution condition fields corresponding thereto have a description of 'CC=000'. Further, in the CD field 404 corresponding to the sub-instruction I01, an offset value '20' is described." In plain English, it is operations/sub-instructions such as branch (BRA) instructions that are decoded in instruction decoders 8 and 9, and it is the execution condition field 401 of an operation/sub-instruction encoded with '010' that makes that operation/sub-instruction into a "condition instruction".

The rest of the language of claim 21, "said condition instruction specifying an operation to be executed under a condition and including a field specifying a timing of starting a determination whether the condition is satisfied; and an instruction execution unit starting a determination of the condition on the basis of the field of said condition instruction and executing the operation under the result of the determination", can be readily interpreted by p. 51, lines 11-16 referenced above, by p. 50, lines 18-23 of appellants' specification where it says, "The sub-instruction I01 is a branch instruction BRA for taking a branch to sub-instruction I11 and I12 having a description of a 'loop' when a branch condition that 'flag F0 is false (namely flag F0 holds 0) is satisfied, wherein the branch condition is judged at the time of executing the sub-instructions I41 and I42", and by p. 54, lines 9-21 where it says, "Further, the PC controlling part 13 receives an offset value '20' which is the CD field outputted from the instruction decode unit 2 and the address No. 1000 from the PC, adds these, and holds a result of the addition of the address No. 1020 in its register 32 at the clock t3. The PC controlling part 13 is comparing the value held in the register 32 with the value indicated by the PC. The PC controlling part 13 judges the execution condition of the branch sub-instruction BRA based on a clock cycle at which the address value in the PC is equal to the address value in the

register 32, namely, a CC value held in the register 31 at the clock t7." In plain English, the condition instruction (sub-instruction I01) specifies an operation (a branch instruction BRA) to be executed under a condition (flag F0 holds 0) and the condition instruction (sub-instruction I01) includes a field (CD field 404) containing an offset value '20' which when added to the value of the PC (program counter) address for sub-instruction I01 gives the value stored in register 32 (1020) of the PC controlling part 13. By comparing the value in register 32 to the value in the PC, the instruction execution unit (PC controlling part 13) determines the time (i.e. when PC=1020) to evaluate the state of flag F0 and branch accordingly.

All the limitations of the language of claim 21 are understood and met by reference to passages from appellants' specification referencing only an instruction/sub-instruction/operation (specifically an **instructio** which is a branch BRA). **Where in appellants' original disclosure is the passage telling one of ordinary skill in the art to ignore the portions of appellants' specification just cited by the examiner when interpreting claim 21 and to only make reference to instruction words?**

How does one of ordinary skill understand the meaning and scope of appellants' claim language when appellants' specification points to and supports two differing interpretations for the language of appellants' claims?

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-25 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. The fact that certain capabilities are provided to the invention by the

format of the very long instruction word (VLIW) instruction (referenced as instruction word by appellants in their appeal brief) (appellants' specification, p.4, lines 7-27 and p. 21, line 26 through p. 22, line 6) while other capabilities are provided by the format of the sub-instructions (p. 22, line 7 through p. 23, line 5 and p. 33, line 26 through p. 41, line 12) of the VLIW instruction is critical or essential to the practice of the invention but not included in the claim(s), and omitting it is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

Appellants' claims mix the capabilities of instructions and sub-instructions without distinguishing as to what provides the capabilities and implying appellants have some form of hybridized instructions which are not enabled.

In response, appellants argue on page 15 (paper no. 23, filed 5/6/02) that "their invention is not limited to the dual instruction having two operations (i.e. sub-instructions) but also includes the single operation instruction" and that their "claims are written to encompass both the dual operation instruction and the single operation instruction". Consider first that appellants have offered no definition for the term, "instruction", anywhere in their specification and that they have used the term in multiple inconsistent ways throughout their disclosure as detailed by the examiner in his 35 USC 112, second paragraph rejection, *supra*.

Consider what happens when one of ordinary skill accepts appellants' argument that "their claims are written to encompass both the dual operation instruction and the single operation instruction," and that the examiners insistence their claims must distinguish between the properties of VLIW instructions and sub-instructions and seeks to recreate appellants' invention of claim 1.

First, it would seem one could not build a modern superscalar or VLIW or multithreaded processor which conformed to the limitations of claim 1. If the first instruction to execute is a single operand instruction or sub-instruction represented by appellants' MULHX instruction (multiply with extended precision, p. 38, line 27 through p. 39, line 1), an instruction found in virtually any conventional superscalar or VLIW or multithreaded processor, the decoding and output by the decoder of a first control signal in a first period (claim 1, lines 8-9 of Appendix A) is done in a rather predictable period though some computer companies have used a combination of fast and slow decoders and other gimmicks which make this period variable. However, the duration of the second period is beyond the system designer's control if one measures from the time when the instruction is decoded until when the execution of the instruction completes because modern superscalar, VLIW, and multithreaded processors typically decode instructions and then send the resultant information to what are frequently referred to as reservation stations to await the retrieval of operands and the freeing of the resources necessary to execute the instruction which can vary from immediately to several instruction cycles because of the mix of instructions executing, efficiency of the cache, exceptions, etc. Even just the time to execute a multiplication with extended precision can vary widely from processor to processor depending on the efficiency of the multiplication hardware. So the "second period" represents a highly variable period for which appellants disclosure provides little guidance and when one considers the difference in time between a multiplication with extended precision and a simple integer addition (the multiplication instruction invariably representing several multiples of the time for the addition), the system designer has no guidance to reconcile the widely variant interpretations of

the "second period" when trying to recreate appellants' claimed invention. The whole situation becomes even more complicated for the system designer trying to replicate appellants' invention if one accepts that the first instruction could be equivalent to a dual operation instruction, as appellants argue. The first period could be relatively determinant since the system has two decoders which may work simultaneously thereby limiting the variation in the first period to the issues discussed in relation to the single operation decode. However, the system designer now has no guidance as to how one calculates the second period for a dual operation instruction. Is it the sum of the execution periods for the two operations or the largest or the smallest, etc? It sure seems like appellants, by insisting there is no limitation to the term instruction and by refusing to narrow it in any way, are forcing ambiguity on the system designer which renders him unable to recreate their invention (i.e. they have a 112, 1st problem), but appellants are entitled to assert what their interpretation of their claims is even if it renders them unpatentable. With the second period indeterminate based on the insufficiency of appellants' disclosure and their repeated insistence an instruction shall be interpreted as any form of instruction, the starting time for the fourth period, defined for the systems designer as "being started after elapsing a same time as said second period or longer from an ending of said third period" (claim 1, lines 18-20), becomes indeterminate (i.e. one of ordinary skill doesn't know how to recreate appellants' invention).

Where in appellants' specification do they provide information which would make these periods determinate quantities?

Appellants' other claims have similar problems based on the ambiguity of terms such as instruction and period.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-25 are rejected under 35 U.S.C. 102(a) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Holmann et al. (Japanese Application No. JP08203675).

As noted in the examiner's previous actions, appellants' severe 112 problems make it unclear how to best apply Holmann. However, despite these problems, the examiner will attempt to point out relevant anticipation and obviousness aspects of Holmann.

Using pseudocode the examiner will provide a small loop-execution program making use of the capabilities of Holmann's delayed branching instructions as set forth in his specification. Since a U.S. application is being examined, the examiner will use the U.S. Patent No. 5,815,698 as a translation of the specification and drawings of JP08203675 though it should be made clear this rejection relies upon the Japanese document being provided to appellants and on its earlier publication date of 2/20/98.

PSEUDO CODE PROGRAM

I1 Move Value to Counter (cols. 11 and 12)

I2 Move Ix to REG1 (cols. 11 and 12)

I3 BSET RP (i.e. make RP valid) (cols. 11 and 12 and col. 18, lines 45-60)

I4 DBRA When PC=REG1 to I4 (cols. 11 and 12 and col. 14, lines 10-20)

I5 Perform Computations

I6 Perform Computations, etc.

Ix-3 Subtract 1 from Counter (cols. 11 and 12)

Ix-2 BRATNZ to Ix testing Counter (cols. 11 and 12)

Ix-1 BCLR RP (i.e. make RP invalid) (cols. 11 and 12 and col. 18, lines 45-60)

Ix Further Processing...

The program performs a loop the number of times set initially in Counter using the DBRA instruction which branches back to itself when the PC equals the address of instruction Ix. It does this as long as the condition RP=1 holds. When the condition changes to RP=0, it does not loop back.

In light of paragraph 19, *supra*, let us consider how Holmann anticipates appellants' claim 14. Holmann certainly has all the hardware of the processing device being claimed (Figs. 5 and 12). He saves the value of the program counter to be used to compare against the PC in a first register (col. 14, lines 25-45) as appellants claim, and the hardware faithfully checks to see if the condition (RP is valid or invalid) as a condition of executing the branch.

As to claim 15, it merely says the value selected to be compared against the PC can be variable which Holmann teaches (col. 20, lines 8-15).

As to claim 16, it fails to teach or define over rejected claims 14-15 in any significant way.

As to claim 18-20, if the conditions of claims 18-20 hold true, then the instruction of claim 14 must inherently be a dual operation instruction and appellants' assertion that it could be a single operation instruction is inconsistent with appellants' specification.

As to claims 21 and 22, they fail to teach or define over rejected claims 14-16.

As to claim 23 and 24, if the conditions of claims 23 and 24 hold true, then the instruction of claim 21 must inherently be a dual operation instruction, and appellants' assertion that it could be a single operation instruction is inconsistent with appellants' specification.

As to how appellants' (for instance) delayed branch-not-equal-to-zero instruction would be obvious to one of ordinary skill in the art, I would again refer to the program of paragraph 19, *supra*. Unless one is an idiot in the art, one recognizes that the code at I4, Ix-2 and Ix-1 is a clumsy way to control the loop. If one makes the BRATNZ instruction capable of delayed operation, one eliminates two instructions thereby reducing the amount of code and speeding execution of the loop. Holmann taught delayed unconditional branching (col. 12). It would be self-evident to one of ordinary skill extending that teaching to include delayed conditional branching would afford greater programming flexibility and would allow reduction in the number of instructions necessary for control of loops using delayed branching thereby speeding execution and reducing code storage requirements. Holmann already taught a dual operand instruction (Fig. 6a). Extending that to allow two delayed operations in the dual operation instruction is merely a logical extension of his concepts. Once one does that then the necessary registers to

hold the appropriate data are necessary for the concept to work and represent no inventive concept.

As to appellants' claims 1-13 and 17, they, too, would then be rendered either obvious or anticipated were they not so ambiguous.

The subject matter of this application admits of illustration by a drawing to facilitate understanding of the invention. Applicant is required to furnish a drawing under 37 CFR 1.81. No new matter may be introduced in the required drawing.

In claims 14, 18, and 20 appellants make many determinations based on the data in registers and other elements and describe a specific sequence of events and timing relationships based on the data and determinations. The same holds true for other of their claims. Appellants have pointed out how parts of several drawings in conjunction with much of their specification will allow one to understand their drawings. The concept behind 37 CFR 1.81 is that the drawing itself, without extensive reference to the specification, will enable understanding of the claim and not that the drawings in conjunction with a 100 page specification will allow understanding of the claim.

The drawings are objected to because they lack suitable legends. 37 1.84(o) states: "Suitable descriptive legends may be used subject to approval by the Office, or **may be required** by the examiner where necessary for understanding of the drawing. They should contain as few words as possible." Appellants drawings contain roughly 46 registers only designated by numbers. Numbers convey no meaning in terms of the drawings elements relevance to any claim language. Without a search through appellants' specification the registers are just numbered

blank boxes in a drawing with no known purpose. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the material set forth in the examiner's previous actions as well as that designated in paragraph 29, *supra*, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

37 CFR 1.83 reads as follows:

§ 1.83 Content of drawing.

(a) The drawing in a nonprovisional application **must show every feature** of the invention specified in the claims. However, conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a labeled rectangular box).

(b) When the invention consists of an improvement on an old machine the drawing must when possible exhibit, in one or more views, the improved portion itself, disconnected from the old structure, and also in another view, so much only of the old structure as will suffice to show the connection of the invention therewith.

(c) **Where the drawings in a nonprovisional application do not comply with the requirements of paragraphs (a) and (b) of this section, the examiner shall require**

such additional illustration within a time period of not less than two months from the date of the sending of a notice thereof. Such corrections are subject to the requirements of § 1.81(d).

[31 FR 12923, Oct. 4, 1966; 43 FR 4015, Jan. 31, 1978; paras. (a) and (c) revised, 60 FR 20195, Apr. 25, 1995, effective June 8, 1995]

Appellants should note that the only provision for not providing a drawing depicting each claim element is when the elements are conventional (i.e. prior art). If appellants are prepared to argue that all claim elements not shown in their drawings, such as the determinations based on the various conditions being claimed, are prior art, the examiner would certainly drop the objection under 37 CFR 1.83(a).

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objections to the drawings will not be held in abeyance.

(11) Response to Argument

In response to the examiner's 35 USC 112, first and second paragraph rejections appellants offer a lot of verbiage without addressing the issues raised by the examiner. If appellants will directly answer the questions the examiner typed in bold letters and underlined, their response will be much more relevant to the rejection.

In response to the examiner's art rejection appellants merely assert Holmann does not teach various aspects of their invention without addressing the examiner's specific arguments made in light of the knowledge of one of ordinary skill.

As to appellants response to the examiner's objections to the drawings, appellants seem to be arguing a blank box with one or more numbers is appropriate because you can find all the stuff in the specification, anyway. **If appellants will explain why passages of the MPEP cited and underlined by the examiner are not applicable to them, it would be instructive.** The examiner finds no such exceptions when he reads the passages.

Unless appellants respond to the specifics of the examiner's rejections and objections, it is hard to be persuaded by appellants' arguments.

-For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

William M. Treat

December 6, 2001

WILLIAM M. TREAT
PRIMARY EXAMINER

Conferees

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